Application number 08/993,442
Amendment dated July 2, 2003
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PATENT

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently amended) An integrated circuit for image frame rendering and DSP applications, the integrated circuit during operation operating with memory, the integrated circuit comprising:

an interface circuit configured to control access to said memory, the interface circuit coupled to said memory;

an embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom; and

an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom and connected to the embedded processor via an internal bus;

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a first shared operand unit coupled to the first MAC unit and the second MAC unit for simultaneously providing a first shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other; and

wherein the array processor further comprises:

a second shared operand unit coupled to a third MAC unit and a fourth MAC unit for providing a second shared operand to the third MAC unit and the fourth MAC unit; and

a shared output and feedback interface coupled to receive the first result from the first MAC unit and the second result from the second MAC unit, and further coupled to provide the first and second results to the first and second local memories.

Claim 2 (Cancelled)

Claim 3 (Previously amended) The integrated circuit according to claim 1 wherein said interface circuit includes a wire bundle for providing wide access data transfers between the interface and said array processor, and wherein said wire bundle comprises at least 256 wires.

Claims 4-9 (Cancelled)

Claim 10 (Currently amended) An integrated circuit using a memory, said integrated circuit comprising:

an interface circuit configured to control access to said memory, said interface circuit coupled to said memory;

an embedded processor configured to control said integrated circuit, said embedded processor receiving information from said interface circuit; and

an array processor for performing mathematical calculations on data received from said interface circuit and connected to said embedded processor via an internal bus, said array processor comprising:

a plurality of multiplier/accumulator circuits; ~~and~~

a plurality of shared operand circuits coupled to said plurality of multiplier/accumulator circuits for simultaneously providing a shared operand to at least two of said plurality of multiplier/accumulator circuits; and

a shared output and feedback interface coupled to receive outputs from the at least two of the plurality of multiplier/accumulator circuits and to provide them for further processing by the at least two of the multiplier/accumulator circuits.

Claim 11(Previously added) The integrated circuit according to claim 10 wherein said interface circuit includes a wire bundle for providing wide access data transfers between the interface and said array processor, and wherein said wire bundle comprises at least 256 wires.

Claim 12 (Previously amended) The integrated circuit according to claim 10 wherein a first instruction stream and a first data stream is maintained for said array processor, and a second instruction stream and a second data stream is maintained for said embedded processor.

Claim 13 (Previously added) The integrated circuit according to claim 10 wherein separate instruction and data streams are maintained for said embedded processor.

Claim 14 (Previously added) The integrated circuit according to claim 10 wherein said interface circuit is a Master Memory Interface Controller (MMIC) circuit.

Claim 15 (Previously added) The integrated circuit according to claim 10 wherein a multiplier/accumulator circuit of said plurality of multiplier/accumulator circuits comprises a computational unit that multiplies a first operand by a second operand to obtain a result and then adds or subtracts from said result a third operand, wherein said operands are either scalars or vectors.

Claim 16 (Previously amended) The integrated circuit according to claim 10 further comprising:

a global external bus unit for providing an interface to said integrated circuit, said global external bus unit coupled to said embedded microprocessor by a system bus and by a separate dedicated bus.

Claim 17 (Previously added) The integrated circuit according to claim 10 wherein said array processor performs a plurality of vector operations selected from a group consisting of addition of a plurality of vectors and multiplying a vector by a scalar.

Claim 18 (Previously added) The integrated circuit according to claim 10 wherein said array processor is configured to share a plurality of scalar elements among a plurality of vector

components of a vector, wherein a first scalar element of said plurality of scalar elements mathematically operating on a first vector component of said plurality of vector components and a second scalar element of said plurality of scalar elements mathematically operating on a second vector component of said plurality of vector components are calculated in parallel.

Claim 19 (Previously added) The integrated circuit according to claim 10 wherein said array processor uses a simplified IEEE floating point notation which excludes said IEEE floating point exceptions, comprising underflow, overflow, divide by zero, inexact, and invalid.

Claim 20 (Currently amended) The ~~array processor~~ integrated circuit of claim 10 ~~further comprising~~ wherein each of the plurality of shared operand circuits comprise:

a front end unit for determining a fixed point result by performing a fixed point addition or subtraction on a plurality of operands; and

a floating point conversion unit for converting said fixed point result to a first floating point result; ~~and~~

~~a multiplier and accumulator unit for determining a second floating point result by performing a floating point multiplication and then accumulation using at least said first floating point result.~~

Claims 21-22 (Cancelled)

Claim 23 (Currently amended) An integrated circuit comprising:

a first embedded processor;

a first array processor coupled to the first embedded processor;

a first memory interface circuit coupled to the first embedded processor and the first array processor;

a first communication port coupled to the first embedded processor;

a second communication port configured to communicate with the first communication port;

a second embedded processor coupled to the second communication port;

a second array processor coupled to the second embedded processor; and

a second memory interface circuit coupled to the second embedded processor and the second array processor,

wherein the first array processor comprises:.

a first MAC unit coupled a first local memory;

a second MAC unit coupled to a second local memory;

a shared output and feedback interface coupled to receive a first output from the first MAC unit and a second output from the second MAC unit and further coupled to provide the first output and the second output to the first and second local memories.

Claim 24 (Currently amended) The integrated circuit of claim ~~21~~ 23 wherein the array processor further comprises:

~~a first MAC unit coupled a first local memory; and~~

~~a second MAC unit coupled to a second local memory~~

a shared operand circuit coupled to the first MAC unit and the second MAC unit for simultaneously providing a first shared operand to the first MAC unit and the second MAC unit.

Claim 25 (Currently amended) An integrated circuit comprising:

a first embedded processor;

an array processor coupled to the first embedded processor;

a memory interface circuit coupled to the first embedded processor and the array processor;

a first communication port coupled to the first embedded processor,

wherein the array processor comprises:

a first MAC unit coupled to a first local memory;

a second MAC unit coupled to a second local memory;

a shared output and feedback interface coupled to receive a first output from the first MAC unit and a second output from the second MAC unit and further coupled to provide the first output and the second output to the first and second local memories; and

a shared operand unit coupled to the first MAC unit and the second MAC unit, the shared operand unit for simultaneously providing a shared operand to the first MAC unit and the second MAC unit.

Claim 26 (Currently amended) The integrated circuit of claim ~~23~~ 25 wherein the first communication port communicates with a second communication port, the second communication port coupled to a second embedded processor.

Claim 27 (New) An integrated circuit comprising:

an interface circuit configured to receive data from an external memory;

an embedded processor configured to control the interface circuit;

an array processor configured to receive data from the interface and to perform arithmetic calculations, the array processor comprising:

a first MAC unit configured to receive data from a first local memory;

a second MAC unit configured to receive data from a second local memory; and

a first shared output and feedback circuit configured to receive data from the first MAC unit and the second MAC unit, and further configured to provide data to the first local memory and the second local memory.

Claim 28 (New) The integrated circuit of claim 27 wherein the array processor further comprises:

a first shared operand circuit configured to simultaneously provide a shared operand to the first MAC unit and the second MAC unit.

Claim 29 (New) The integrated circuit of claim 28 further comprising:

a communication port coupled to the embedded processor.

Claim 30 (New) The integrated circuit of claim 29 wherein the array processor further comprises:

a third MAC unit configured to receive data from a third local memory;

a fourth MAC unit configured to receive data from a fourth local memory;

a second shared output and feedback circuit configured to receive data from the third MAC unit and the fourth MAC unit, and further configured to provide data to the first local memory, the second local memory, the third local memory, and the fourth local memory; and

a second shared operand circuit configured to simultaneously provide a shared operand to the third MAC unit and the fourth MAC unit.